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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,200	01/11/2006	Takashi Kariya	282371US90PCT	7428
22850	7590	02/01/2007	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			ABRAMS, NEIL	
1940 DUKE STREET			ART UNIT	PAPER NUMBER
ALEXANDRIA, VA 22314			2839	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/01/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/564,200	KARIYA ET AL.
	Examiner	Art Unit
	Neil Abrams	2839

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 1-11-06 (prelim amdt)
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-9 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-9 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1) Certified copies of the priority documents have been received.
 2) Certified copies of the priority documents have been received in Application No. _____.
 3) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Applicant asked to provide any available information as to teachings of cited Japan patent 59-996. Does it refer to resin substrate or to Youngs modulus? Claim 8 objected to; line 2 should read --- ...of said through holes... ---lines 3,4 should read ---....the holes in the center of the through holes ---

1. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azuma in view of Turlik, Farooq , Ikeda, Uchikawa, Milkovich and Japan 59-996.
2. For claim 1, Azuma, figure 1 discloses an interposer 2 between an IC chip 11 and a package substrate 3 made of resin, col 6, lines 21-23, and with through hole conductors at 23. The claim 1, line 6 relationship seems so wide as to be readily met by most systems and is also met by by Azuma as depicted .

Azuma lacks the claim 1 Youngs modulus relationship. Ikeda discloses use of a ceramic interposer at 6 used between chip 1 and wiring board 9 , ceramic modulus being in range recited in claim 1. . Farooq at column 4, lines 50-55, teaches use of a ceramic interposer with a modulus greater than about 50 Gpa. . Turlik, column 6, lines 45-60 refers to interposer 12 with modulus of 410 Gpa and 300 Gpa. Obvious to use any such type low expansion materials for Azuma interposer to lessen thermal mismatch with the chip , see Turlik, column 2, lines 65-68. Milkovich added for (about 360 Gpa) statement of ceramic modulus of 53 Mpsi which meets claim 1 limitation in this regard . Ikeda dos not refer to modulus , but apparent that it would be in of similar value .

Claim 3 clearly met by Azuma , as modified. Claims 6, 7, use of plated holes and of

metallic paste in holes is standard in the circuit board art. Also Azuma fill material at

23 seen to meet claim 7. For claim 1, Farooq "greater than 50 Gpa" seen to fall in recited range "55 to 440".

3. For claims, 2, 5, 9, Azuma lacks a multilayer pcb or a pcb core. Uchikawa, figure 1 uses a multilayer pcb with a core at leadline 2. Japan at 18, 15 appears to use a multilayer pcb and an interposer. Obvious to use either such multilayer type pcb in Azuma to provide increase circuit paths and since this is a standard type of pcb. Claim 2 with "or more" limitation is broadly stated and should be obvious aspect of Azuma used with multilayer Uchikawa type pcb. Claim 4 treated as obvious variation since the recited features are not related to invention objects as set forth in specification. Claim 7 metallic paste also seems taught by Uchikawa at 6E. Obvious to use this feature in Azuma to increase conductivity. Claim 8 with "is equal to" limitation met by Azuma, see holes 23a.

To further support rejection as applied to claim 1, use of resin or glass epoxy resin for pcb or package substrate is seen to be "standard" see Uchikawa, abstract and Milkovich, col 4, lines 50-55.. Farooq, Ikeda and Turlik should be viewed as used with such type pcbs since that is standard manner of use. Also note that Turlik interposer is usable without pins 11, col 7, lines 20-25, hence is analogous to Azuma in this regard.

4. Claims 1,3,4,6,7,8, are rejecter under 35 USC 103(a) as unpatentable over

~~Milkovich~~ Milkovich.

5. For claim 1, Milkovich interposer (top layer) 3 is located between ic chip 31 and substrate or pcb 39 made of epoxy resin and includes conductive through holes 11

and is made of ceramic with elastic modulus in range recited. Since figs are not to scale interposer 3 thickness not clearly disclosed however since line 6 range is very wide it seems obvious that in normal production, interposer 3 thickness would be in recited range especially since lower limit would result in interposer too thin to produce necessary flexibility to avoid damage to solder attachments. This would also be to provide strength to the interposer. Claims 3, 6,7,8 relate to standard expedients that should not be at issue. Claim 4 treated as discussed above.

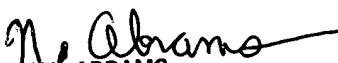
6. Claims 2,5,9 are rejected under 35 USC 103 a as unpatentable over Milkovich in view of Uchikawa.

7. Milkovich lacks multilayer pcb with core. Uchikawa discloses such type substrate with core 2. Obvious to use such type in Milkovich for greater number of circuit paths. Claim 2 feature would be obvious variation since it produces no stated new result over the references as applied .

8. Wojnar, further shows resin to be standard for pcb material, col 2, line 60.

Matsuda, para 0004 also discloses resin for a printed substrate

Any inquiry concerning this communication should be directed to Neil Abrams at telephone number 571-272-2089


NEIL ABRAMS
PRIMARY EXAMINER